

Customer No.: 31561
Application No.: 10/708,016
Docket No.: 12030-US-PA

AMENDMENTS

In The Claims

1. (original) A pixel structure, adapted to be disposed on a substrate, comprising:
a scan line, disposed on the substrate;
a data line, disposed on the substrate;
an active element, disposed near to an intersection of the scan line and the data line on the substrate, and electrically coupled to the scan line and the data line;
a capacitor electrode, disposed on the substrate;
a pixel electrode, disposed over the capacitor electrode and electrically coupled to the active element, wherein the pixel electrode and the capacitor electrode form a pixel storage capacitor; and
an electrical field shielding layer, disposed between the data line and the pixel electrode.
2. (original) The pixel structure of claim 1, wherein the active element comprises a low temperature polysilicon thin film transistor.
3. (original) The pixel structure of claim 2, further comprising a drain/source conductive layer, wherein the active element is electrically coupled to the data line and the pixel electrode through the drain/source conductive layer.
4. (withdrawn) The pixel structure of claim 2, further comprising a conductive layer, wherein the active element is electrically coupled to the data line through the

Customer No.: 31561

Application No.: 10/708,016

Docket No.: 12030-US-PA

drain/source conductive layer, and the pixel electrode is directly electrically coupled to the active element.

5. (withdrawn) The pixel structure of claim 4, wherein the conductive layer is indium tin oxide or indium zinc oxide.

6. (original) The pixel structure of claim 1, further comprising a transparent capacitor electrode, disposed between the capacitor electrode and the pixel electrode, wherein the capacitor electrode, the transparent capacitor electrode and the pixel electrode form the pixel storage capacitor, and the capacitor electrode is made from a transparent material.

7. (original) The pixel structure of claim 6, wherein the active element is directly electrically coupled to the capacitor electrode or the transparent capacitor electrode.

8. (withdrawn) The pixel structure of claim 6, wherein the active element is electrically coupled to the capacitor or the transparent capacitor electrode through the pixel electrode.

9. (original) The pixel structure of claim 6, wherein the transparent capacitor electrode is made from indium tin oxide or indium zinc oxide.

10. (withdrawn) The pixel structure of claim 1, wherein the active element comprises an amorphous silicon thin film transistor.

11. (withdrawn) The pixel structure of claim 10, wherein the active element comprises:

a gate terminal, disposed on the substrate and electrically coupled to the scan line;

a channel, disposed on the gate terminal; and

Customer No.: 31561
Application No.: 10/708,016
Docket No.: 12030-US-PA

a source/drain terminal, disposed on the channel and electrically coupled to the data line and the pixel electrode.

12. (original) The pixel structure of claim 1, wherein the capacitor electrode, the electrical field shielding layer and the pixel electrode are made from indium tin oxide or indium zinc oxide.

13. (withdrawn) A method of fabricating a pixel structure, comprising:
sequentially forming an active element, a scan line and a data line on a substrate, the active element being electrically coupled to the scan line and the data line;
forming a capacitor electrode on the substrate;
forming an electrical field shielding layer on the substrate, covering the data line;
and

forming a pixel electrode on the substrate, covering the capacitor electrode and electrically coupled to the active element, wherein the pixel electrode and the capacitor electrode are coupled as a pixel storage capacitor.

14. (withdrawn) The method of fabricating a pixel structure of claim 13, wherein the electrical field shielding layer and the capacitor electrode are formed by a patterned material layer.

15. (withdrawn) The method of fabricating a pixel structure of claim 13, wherein the active element comprises a low temperature polysilicon thin film transistor.

16. (withdrawn) The method of fabricating a pixel structure of claim 15, while forming the data line, further comprising forming a source/drain conductive layer over the

Customer No.: 31561

Application No.: 10/708,016

Docket No.: 12030-US-PA

active element, wherein the active element is electrically coupled to the data line and the pixel electrode through the drain/source conductive layer.

17. (withdrawn) The method of fabricating a pixel structure of claim 15, after forming the data line, further comprising a step of forming a conductive layer over the active element, wherein the active element is electrically coupled to the data line through the drain/source conductive layer, and the pixel electrode is directly electrically coupled to the active element.

18. (withdrawn) The method of fabricating a pixel structure of claim 17, wherein the conductive layer and the pixel electrode are formed from a patterned material layer.

19. (withdrawn) The method of fabricating a pixel structure of claim 15, wherein the step of forming the active element comprises:

forming a polysilicon layer on the substrate;

forming a gate dielectric layer on the substrate, covering the polysilicon layer;

forming a gate terminal on the gate dielectric layer and over the polysilicon layer;

and

forming a source/drain doped region within the polysilicon layer besides the gate terminal.

20. (withdrawn) The method of fabricating a pixel structure of claim 19, wherein the step of forming the source/drain doped region comprises performing a doping process using the gate terminal as a hard mask for forming the source/drain doped region.

21. (withdrawn) The method of fabricating a pixel structure of claim 13, wherein the active element comprises an amorphous silicon thin film transistor.

Customer No.: 31561
Application No.: 10/708,016
Docket No.: 12030-US-PA

22. (withdrawn) The method of fabricating a pixel structure of claim 21, wherein the step of forming the active element comprises:

forming a gate terminal on the substrate, electrically coupled to the scan line;
forming a gate dielectric layer on the substrate, covering the gate terminal;
forming a channel on the gate dielectric layer and over the gate terminal; and
forming a source/drain terminal on the channel.

23. (withdrawn) The method of fabricating a pixel structure of claim 13, after forming the capacitor electrode and before forming the pixel electrode, further comprising a step of forming a transparent capacitor electrode on the capacitor electrode.

24. (withdrawn) The method of fabricating a pixel structure of claim 23, wherein the capacitor electrode or the transparent capacitor electrode is formed along with the electrical field shielding layer by a patterned material layer.

25. (withdrawn) The method of fabricating a pixel structure of claim 13, wherein the capacitor electrode, the electrical field shielding layer and the pixel electrode are made from indium tin oxide or indium zinc oxide.